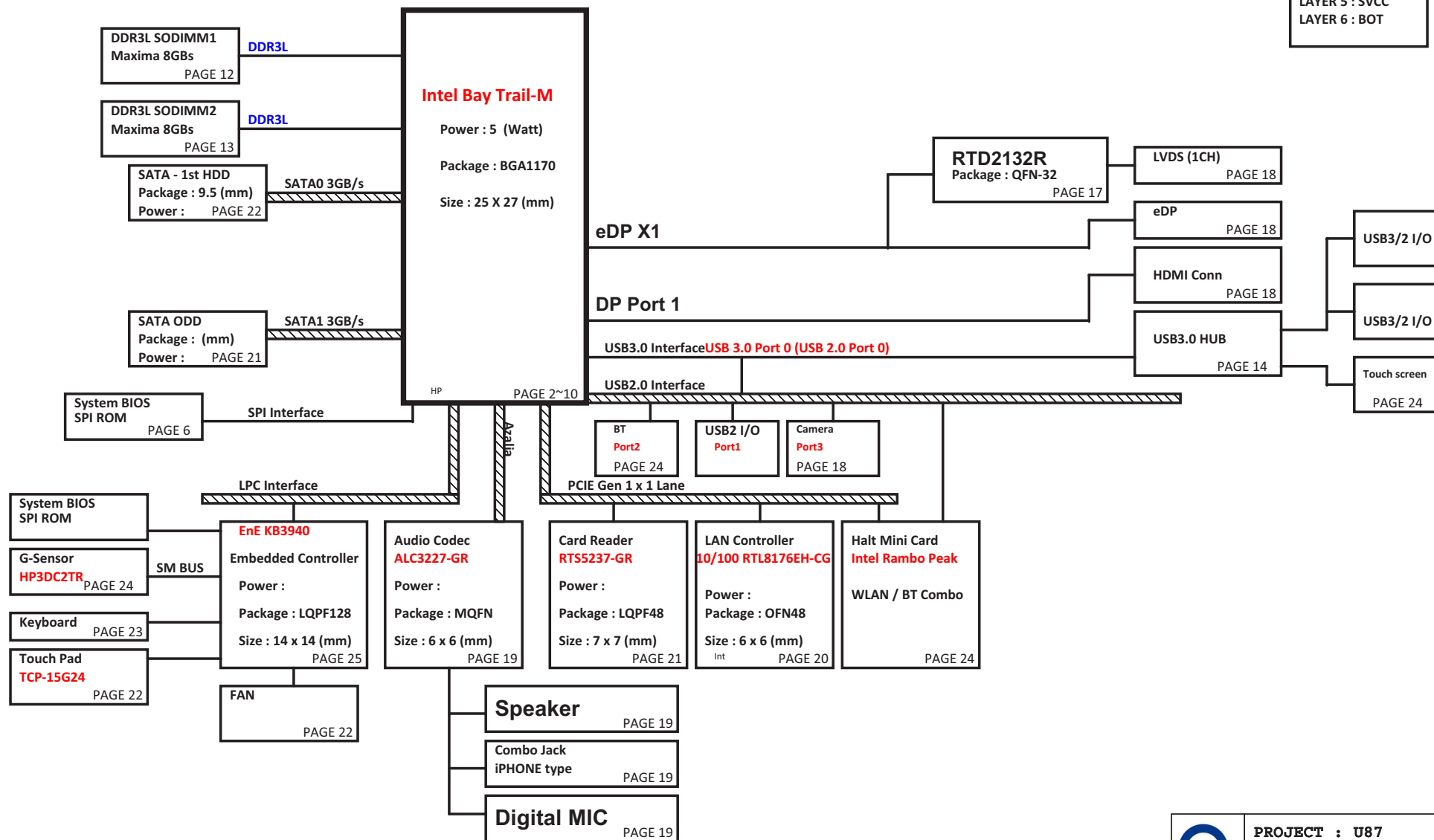
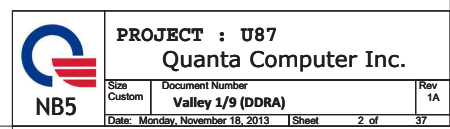


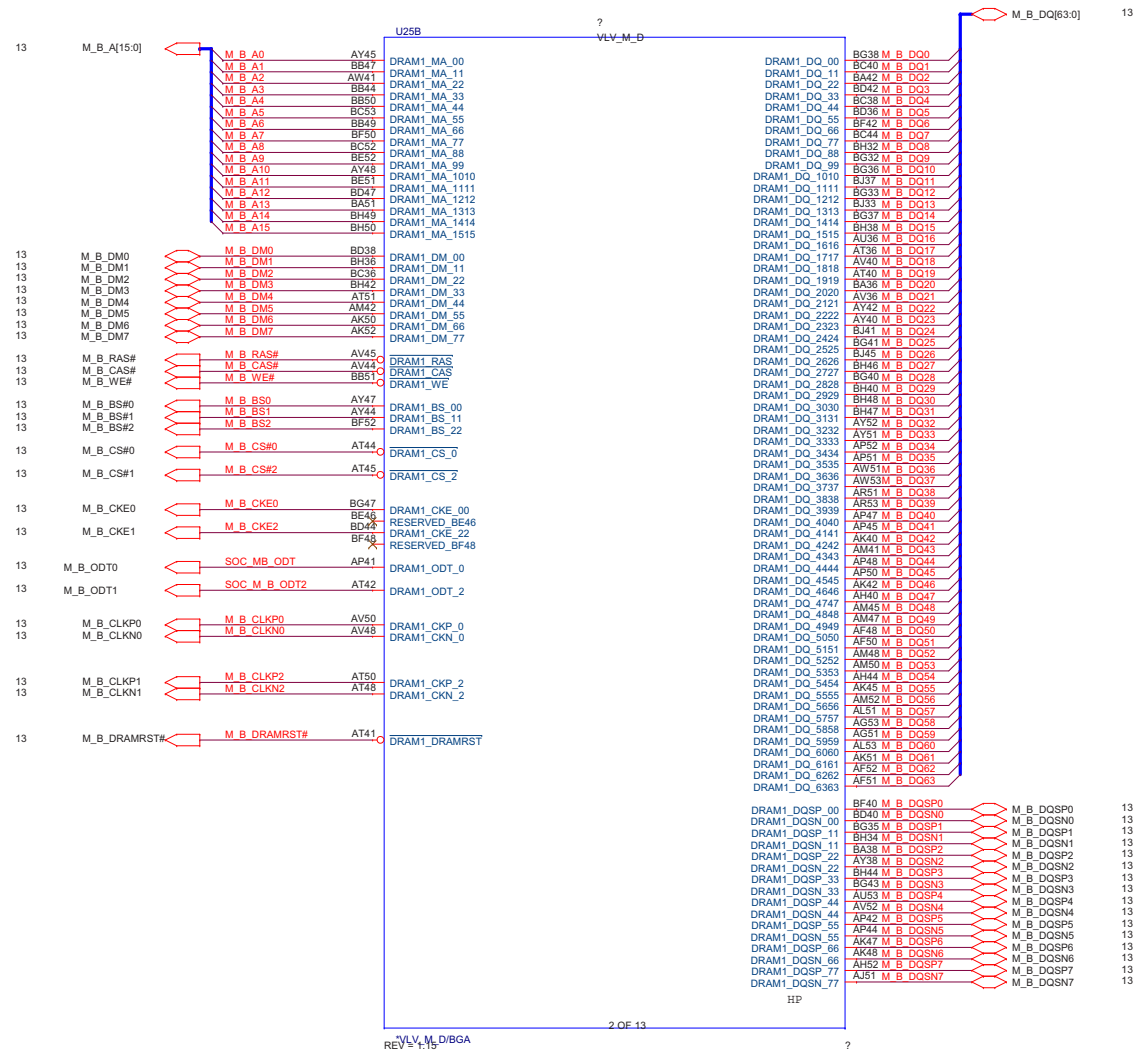
U87/U88 UMA (14"/15.6") Ultra/Slim Intel Bay trail-M Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

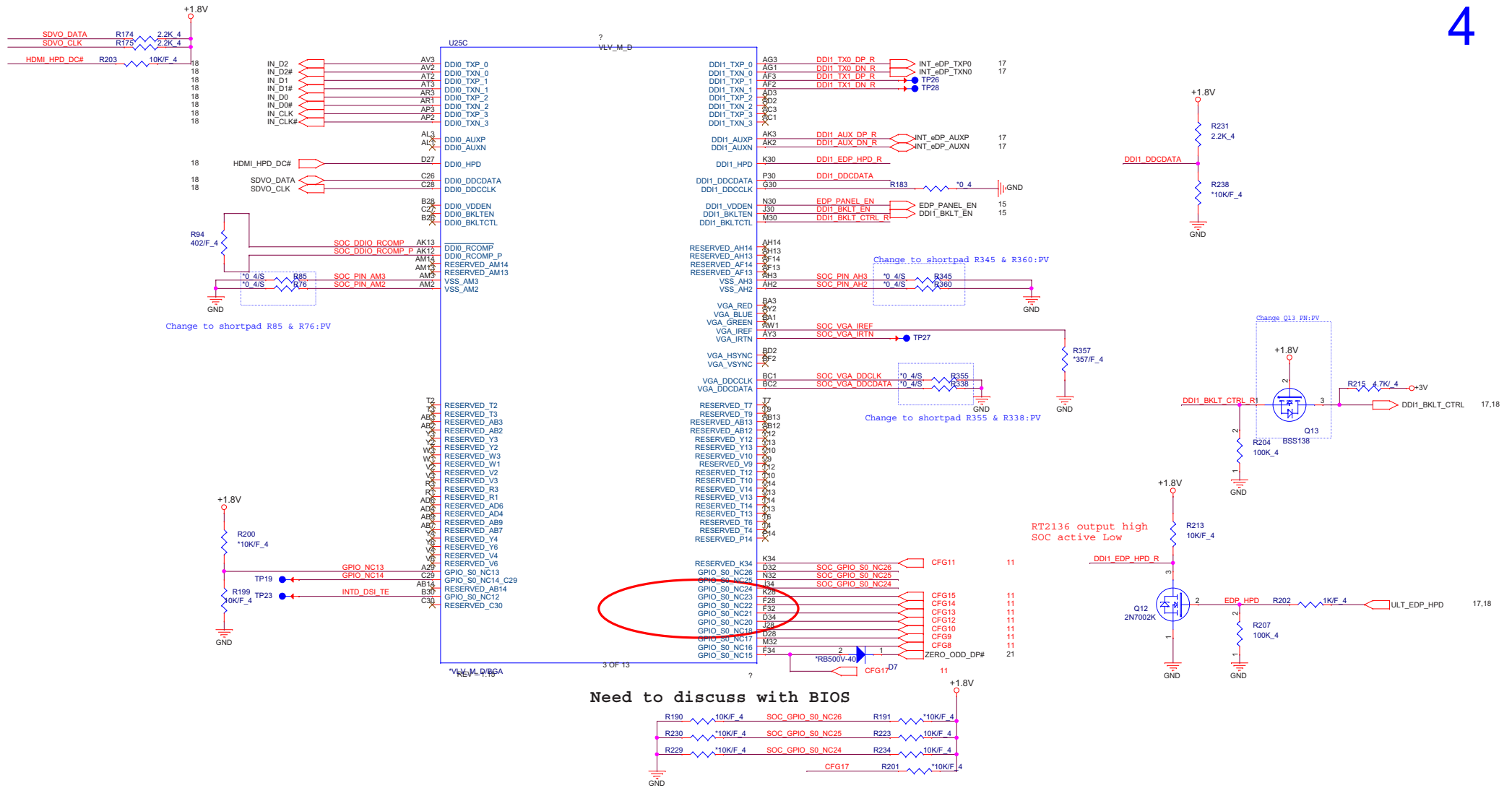






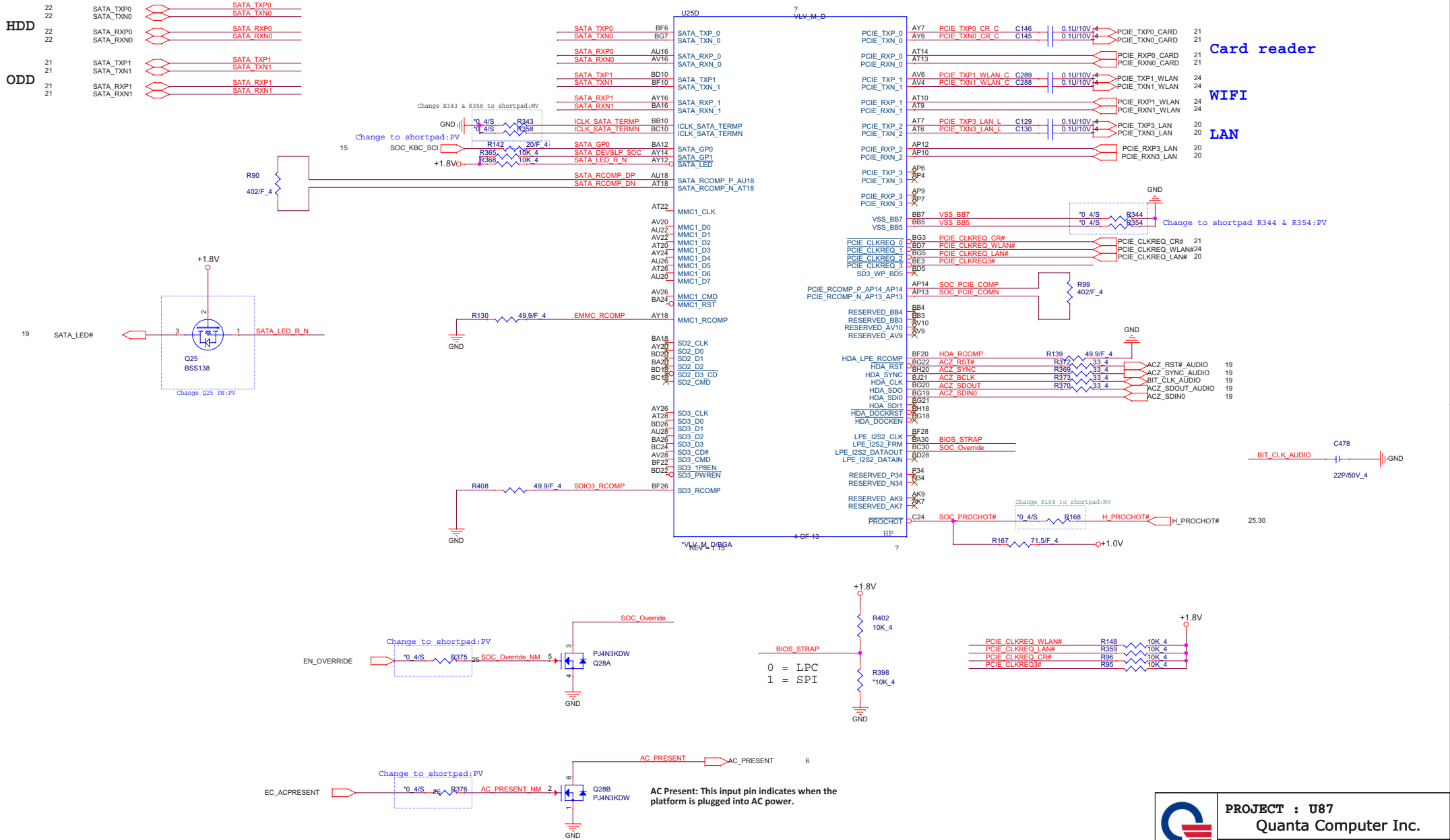
PROJECT : U87
Quanta Computer Inc.

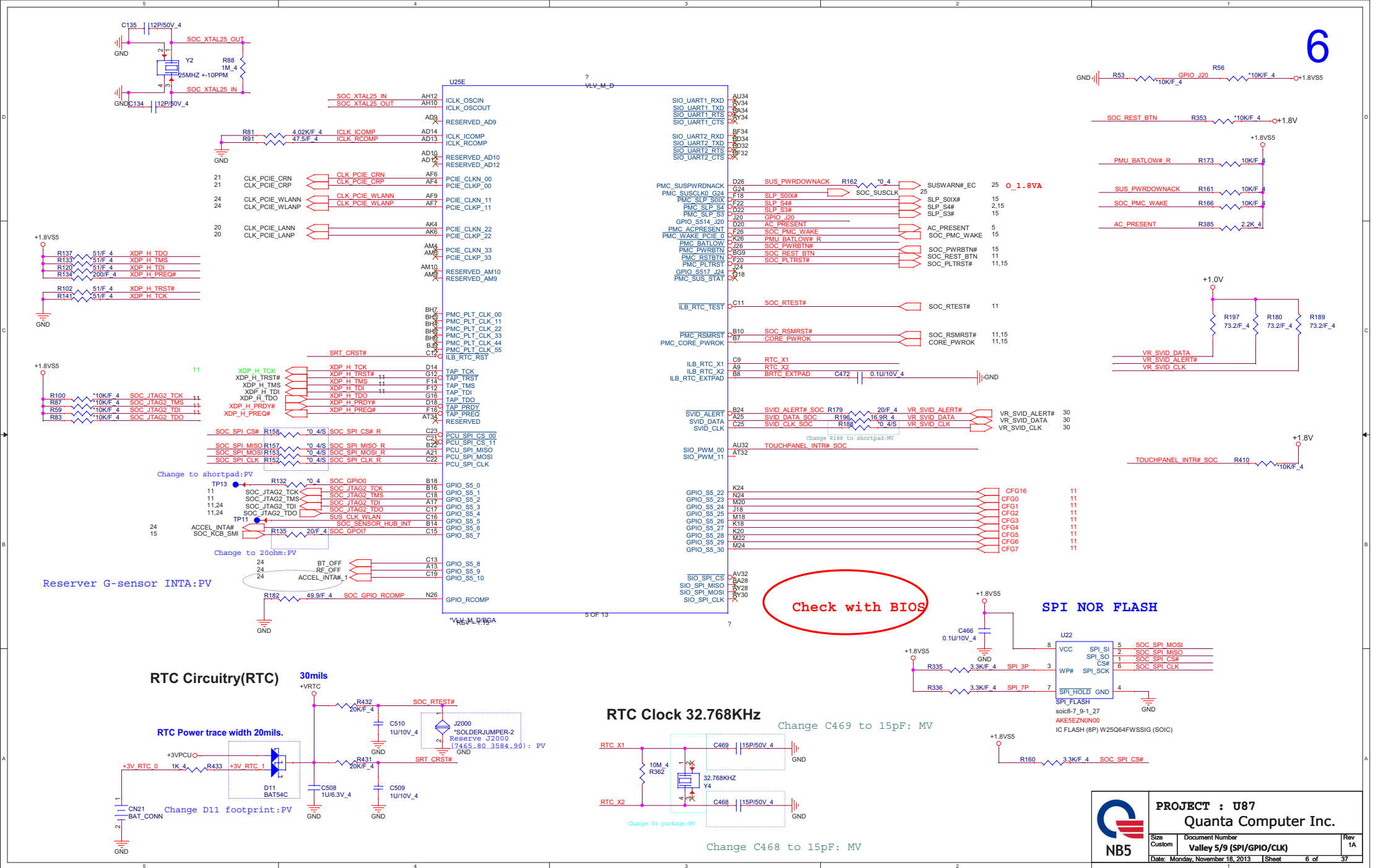
Size	Document Number	Rev
Custom	Valley 2/9 (DDR8)	1A
Date: Monday, November 18, 2013	Sheet 3 of 37	

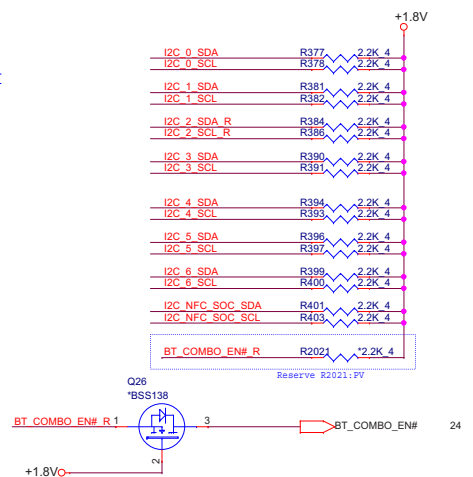
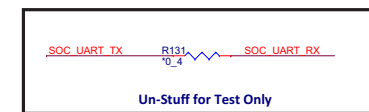
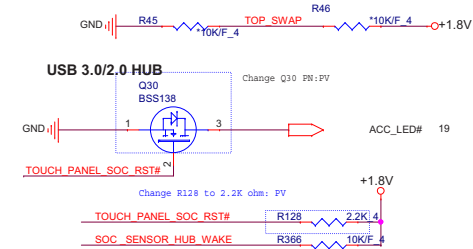


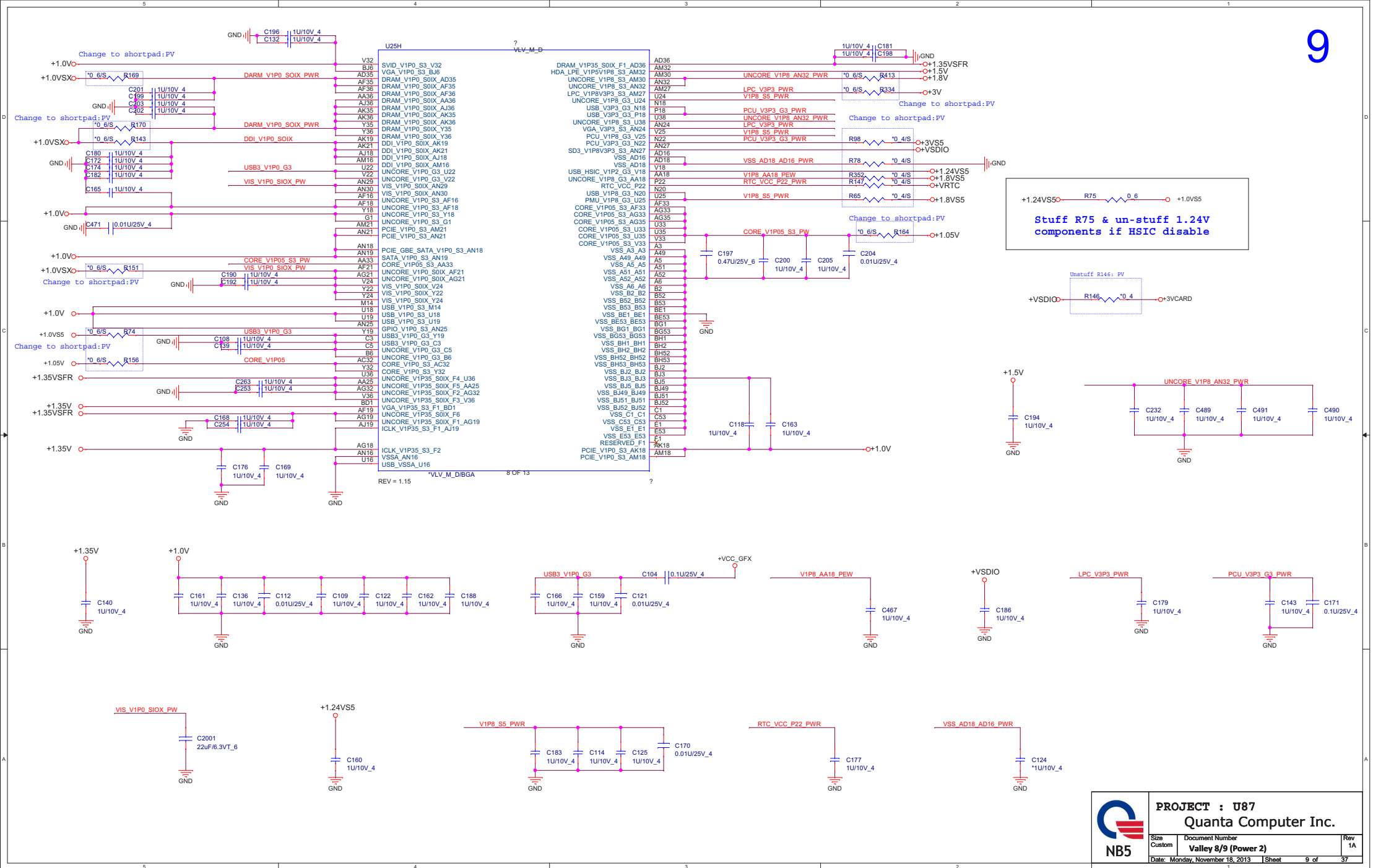
Need to discuss with BIOS

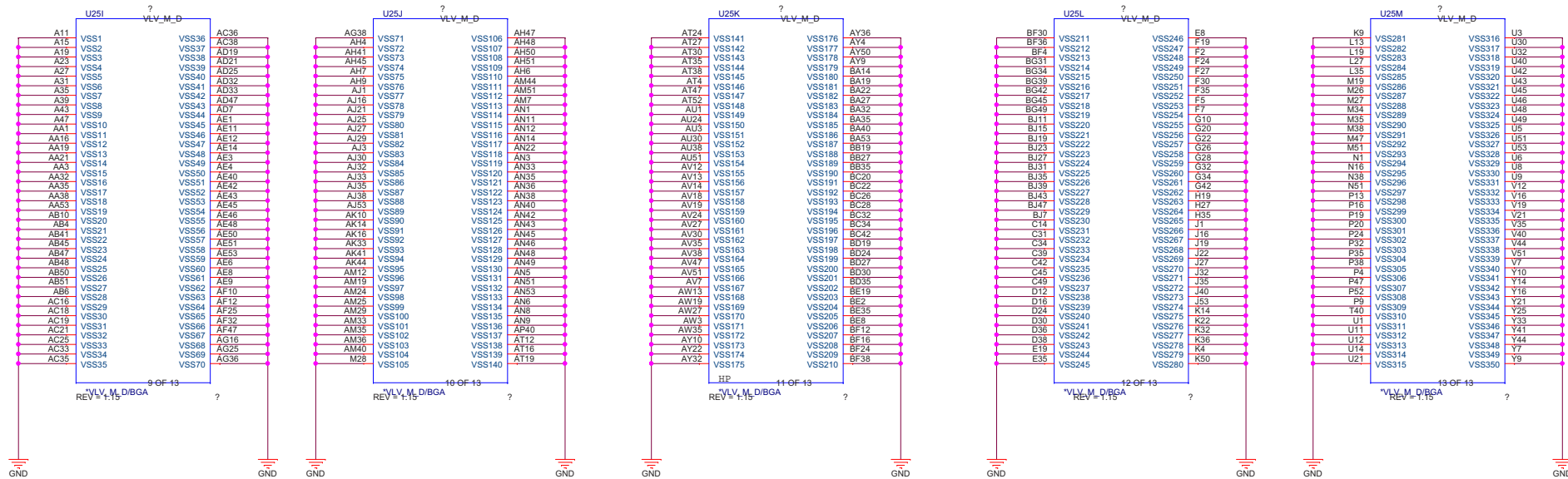
GPIO26	0	0	
GPIO25	0	0	0=HDD+ODD, 1= eMMC only
GPIO24	0	1	0=14 ", 1=15 "

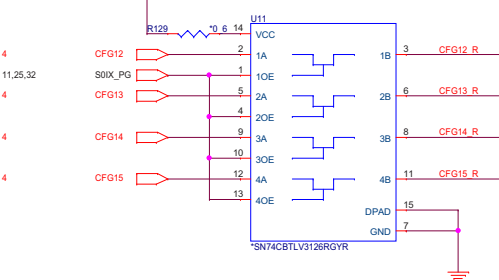
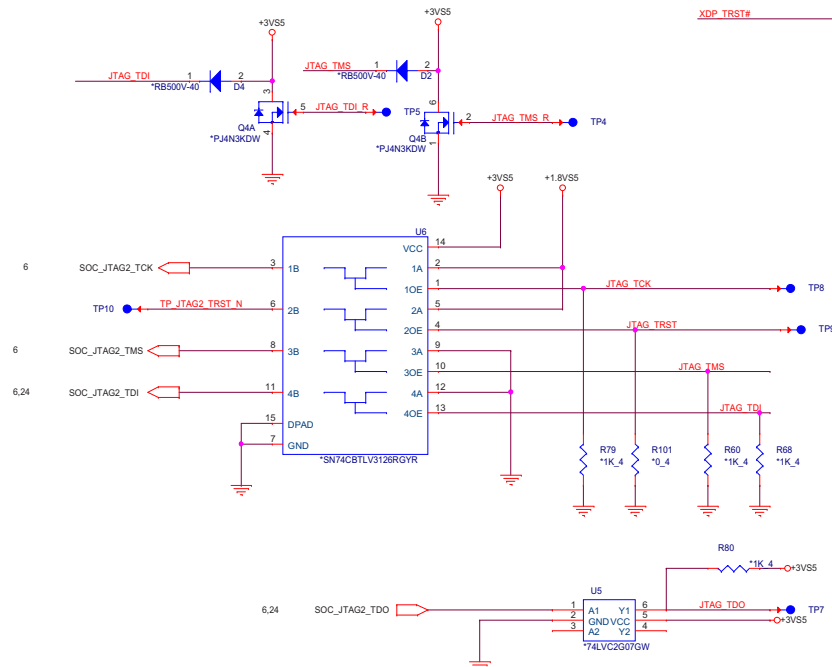


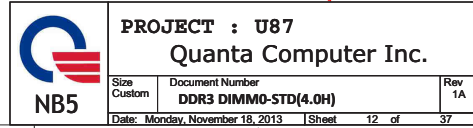
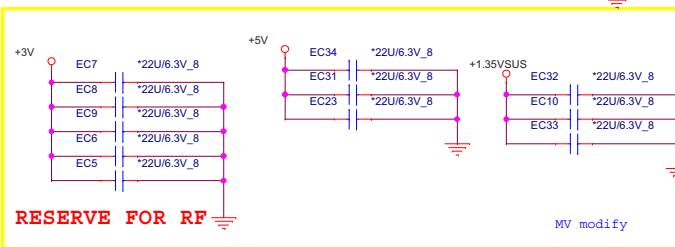


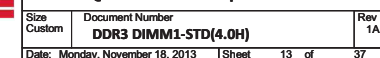
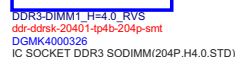


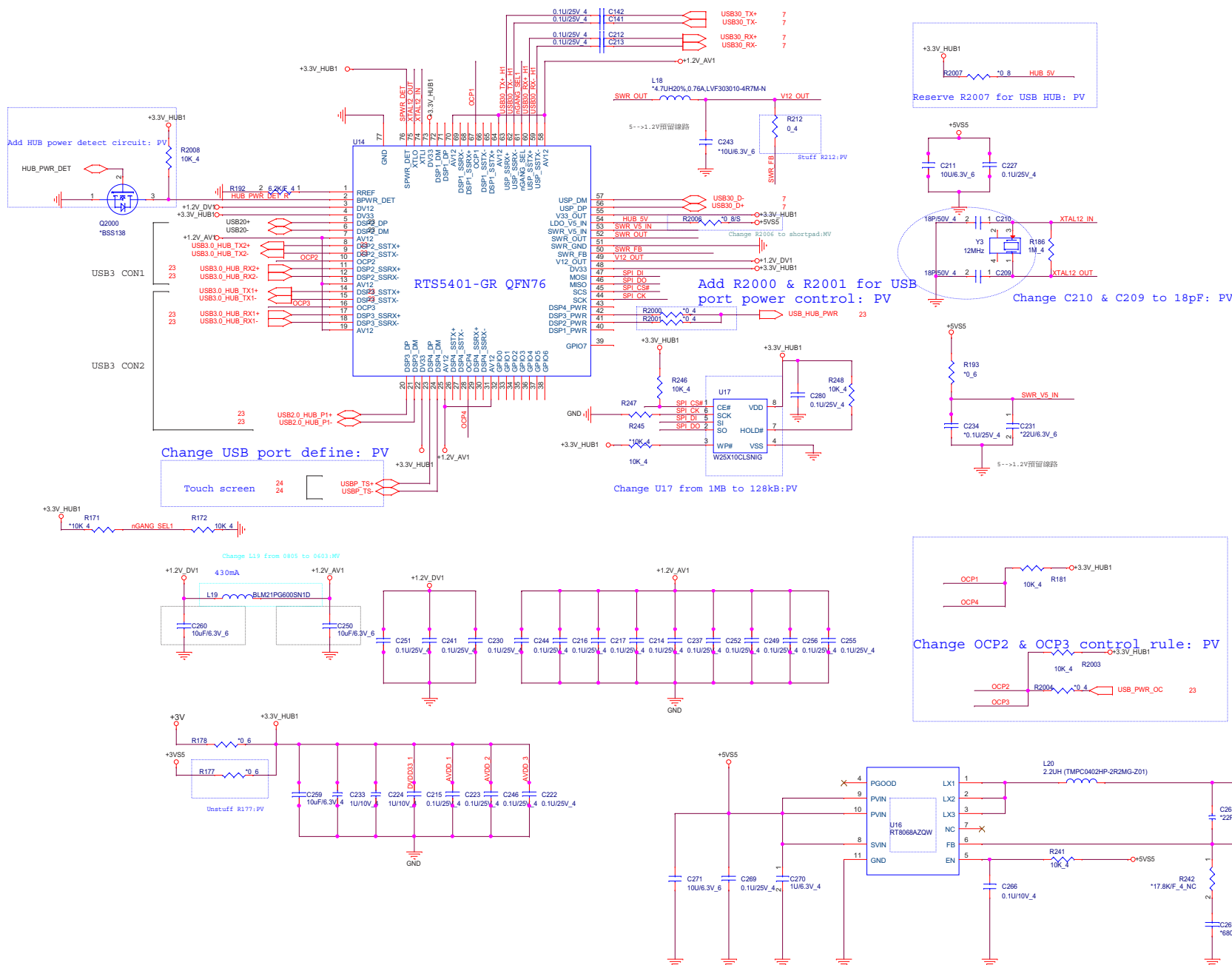


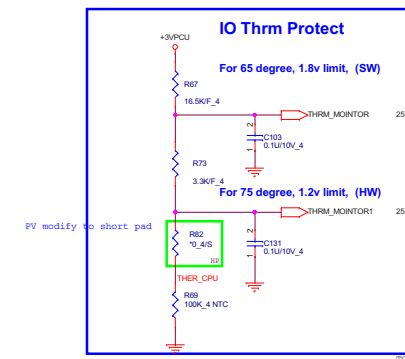
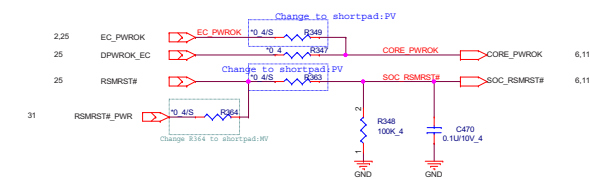
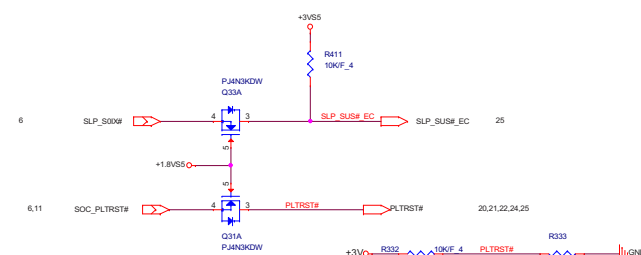
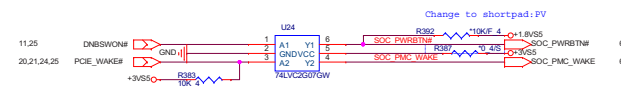
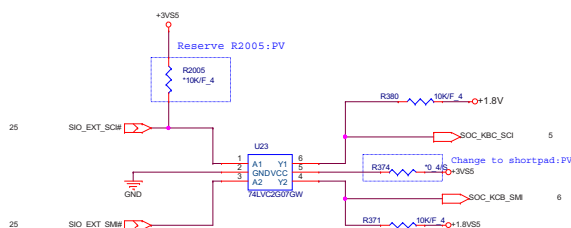
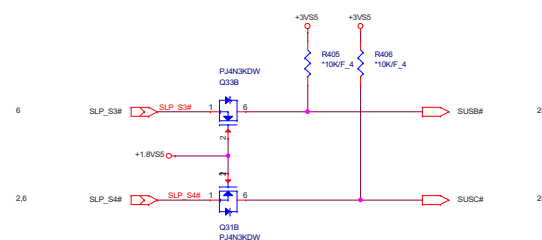
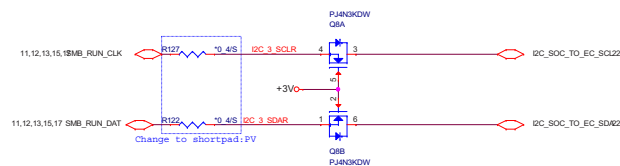
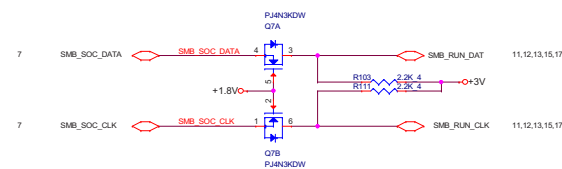
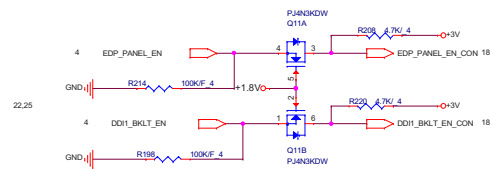
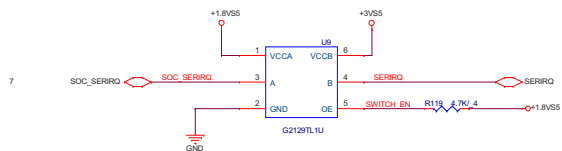












S5 to S0 Cold Boot Sequence without S0ix

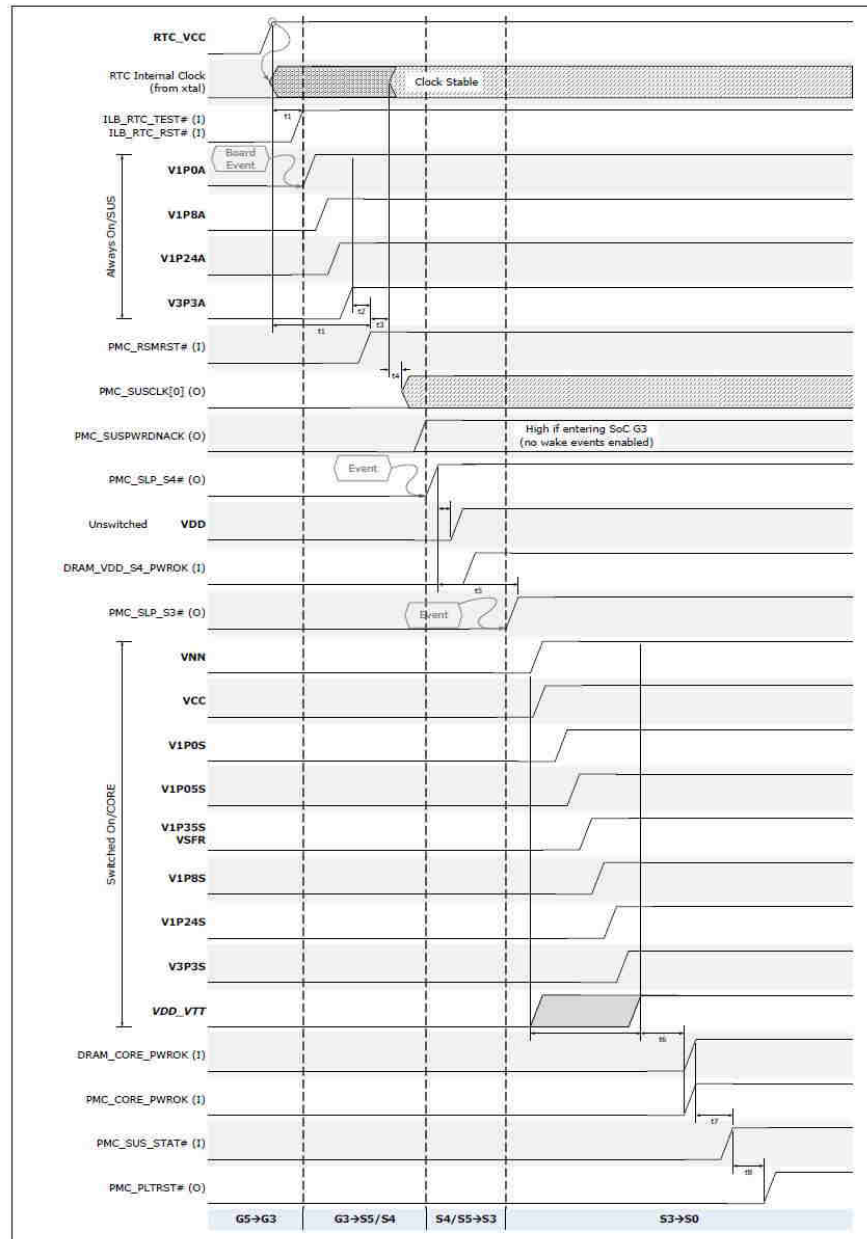


Table 4-12. Cold Boot Timing Spec

Parameter	Description	Min	Typ	Max	Units
T0	RTC_VCC stable to ILB_RTC_TEST# high	9			ms
T1	VR ramp up time from 10% to 90% voltage level			2	ms
T2	Rail to subsequent rail turn on delay	10		2000	us
T3	VSUS stable to PMC_RSMRST# high	10			ms
T4	S and SX rails stable to PMC_CORE_PWROK	100			ms

NOTES:

1. T1 and T2 are recommended time for all the VR rails unless specified otherwise. The VR ramp up time T2 and subsequent rail delay T3 are put in place to avoid inrush current which may be caused by multiple loads turning on simultaneously or fast charging of VR output decoupling.
2. Violation of rail-to-rail sequencing may cause the SoC part long term reliability issue.
3. Platform devices other than SoC sequencing are not explicitly shown as they are not limited by the SoC sequencing requirement.



PROJECT : U87
Quanta Computer Inc.

Size C Document Number
Power sequence
Date: Monday, November 18, 2013 Sheet 16 of 37 Rev 1A



3

3



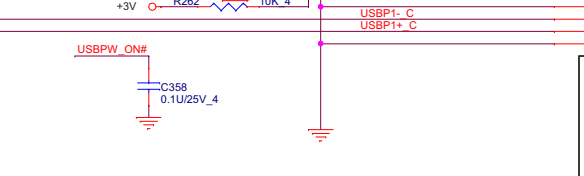
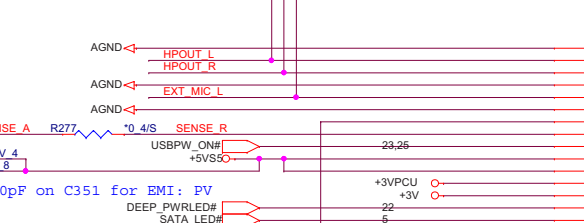
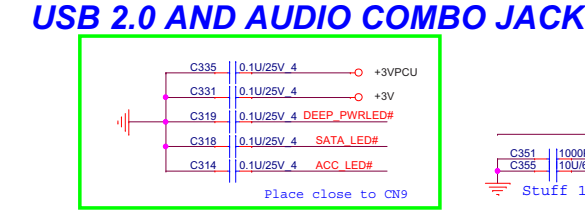
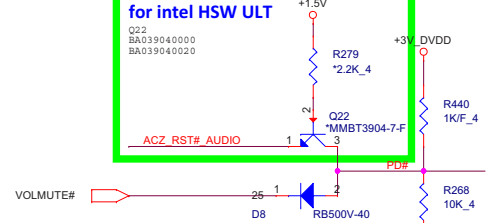
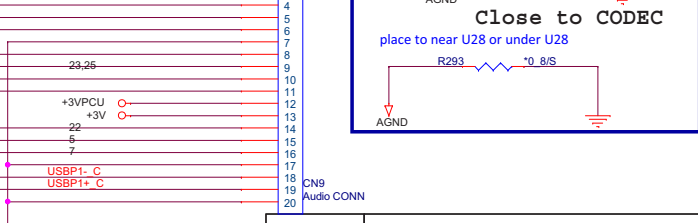
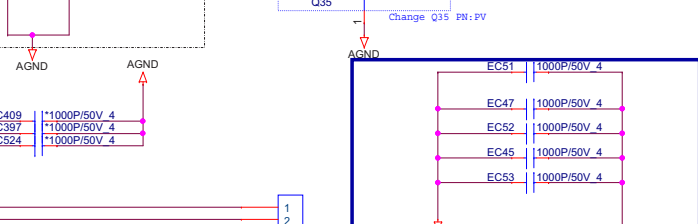
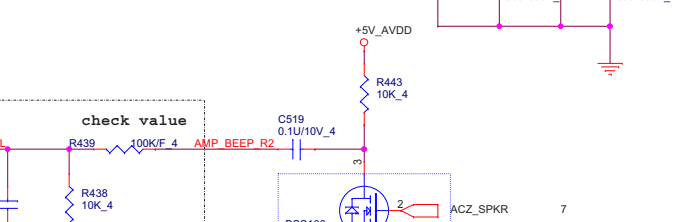
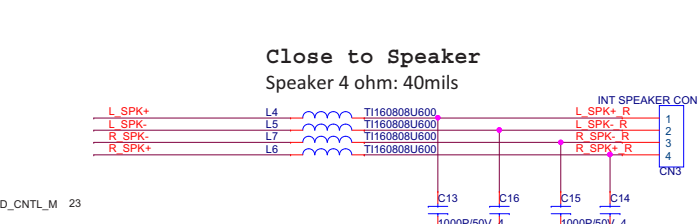
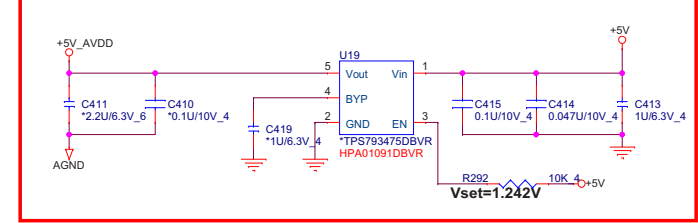
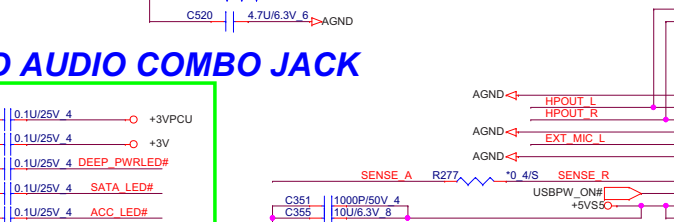
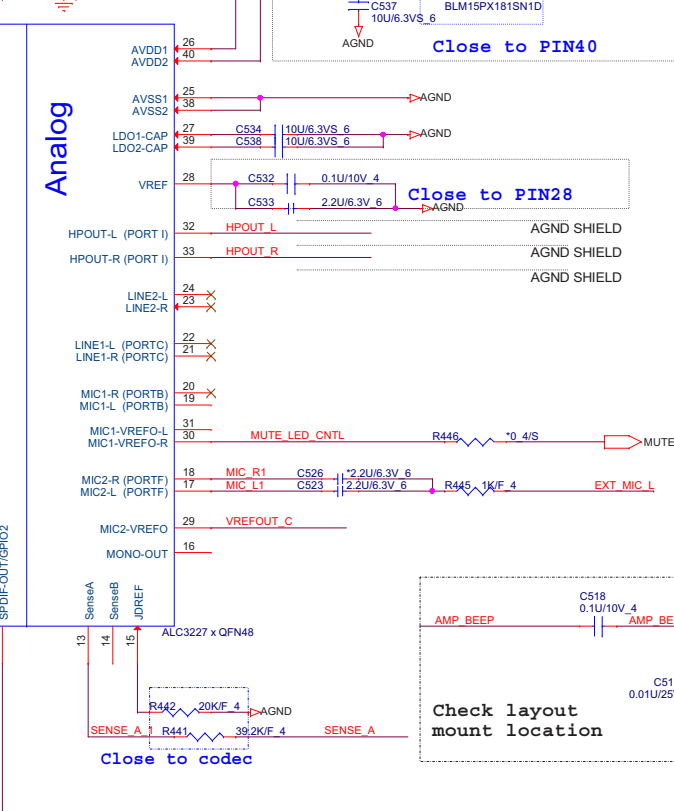
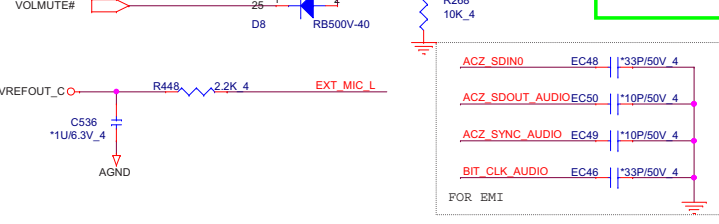
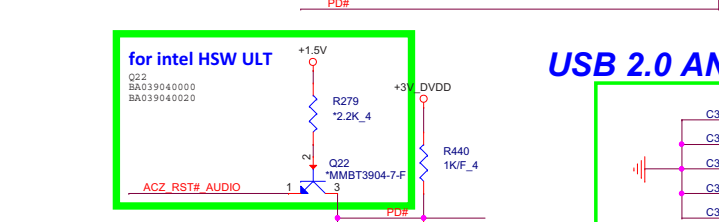
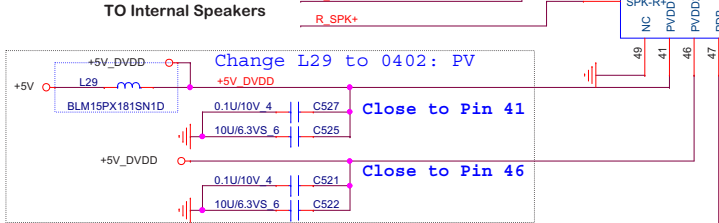
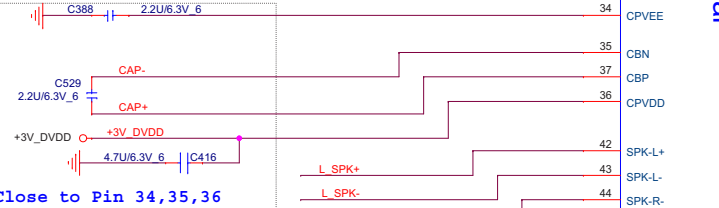
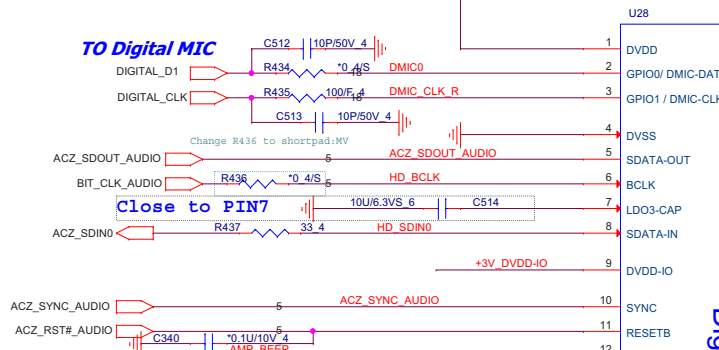
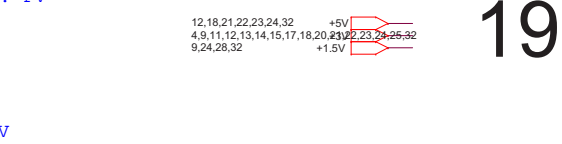
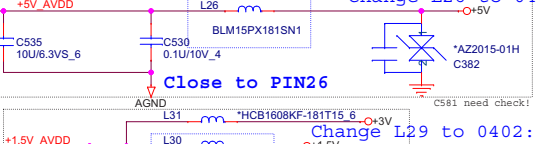
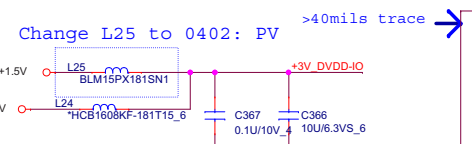
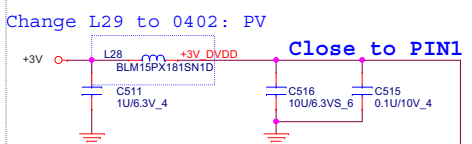
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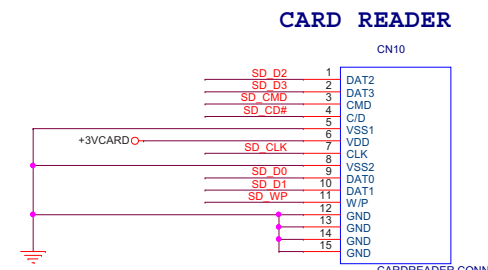
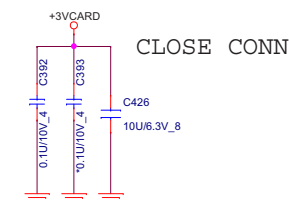
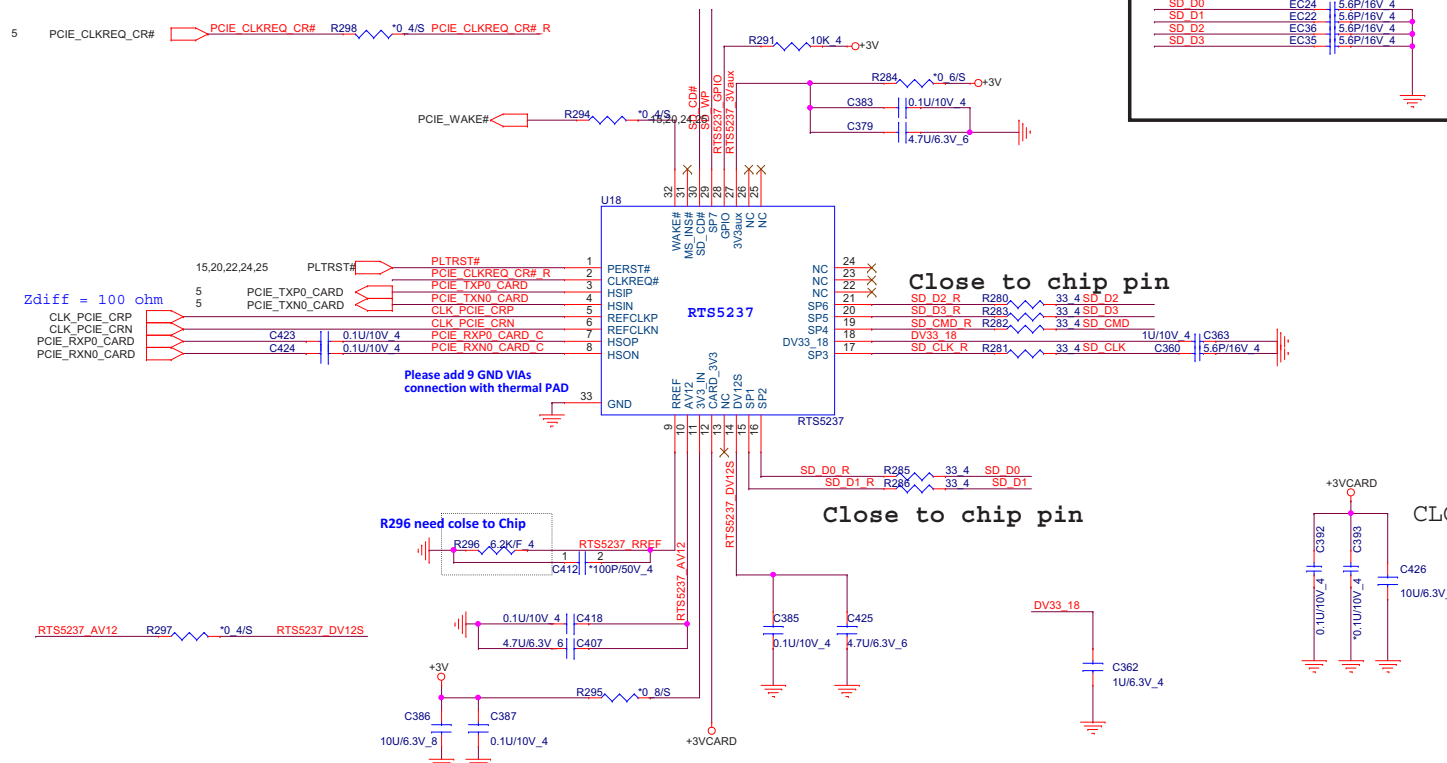


Reserve for EMI

SP1	SD D1	
SP2	SD D0	MS D1
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD WP	MS BS

Share Pin

SD / MMC

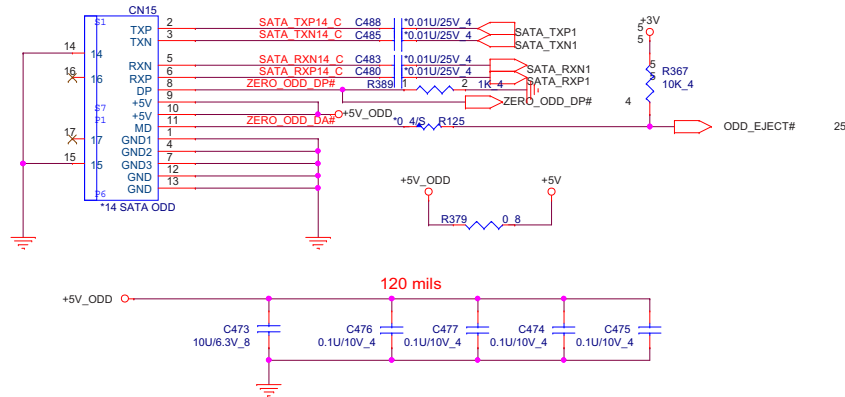


R3X Type

**SATA ODD
CONNECTOR**

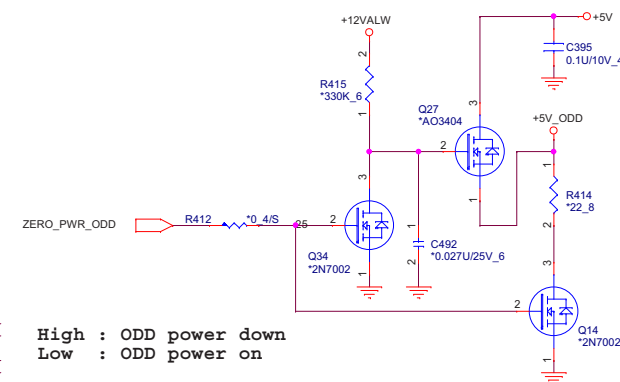
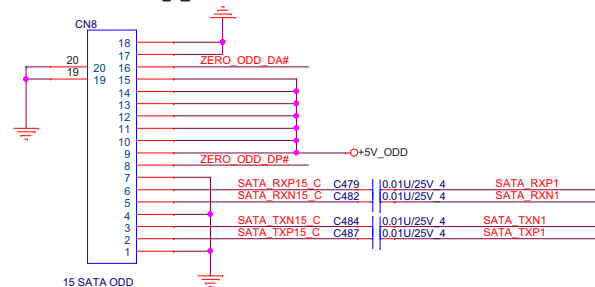
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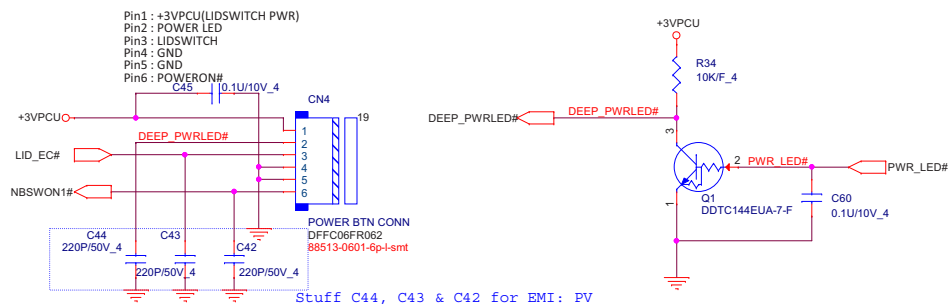


15" SATA ODD

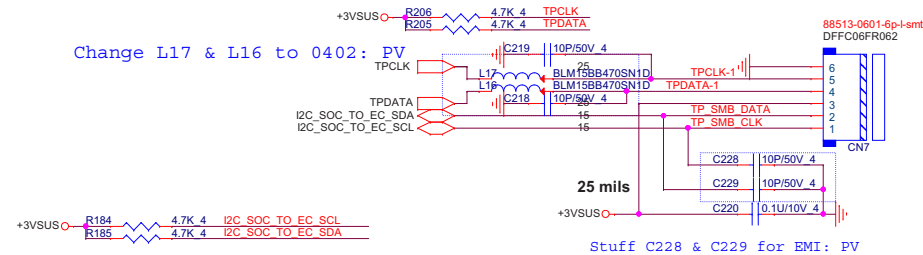
New Type



Power Button Connector



Touch Pad Connector



Change L17 & L16 to 0402: PV

88513-0601-6p-l-sm

DFFC06FR062

TPCLK-1

TPDATA-1

TP SMB DATA

TP SMB CLK

TPCLK-1

TPDATA-1

TP SMB DATA

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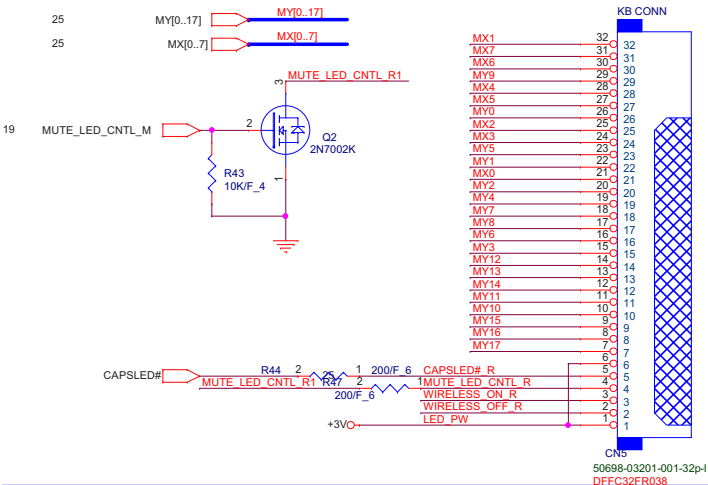
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TPDATA-1

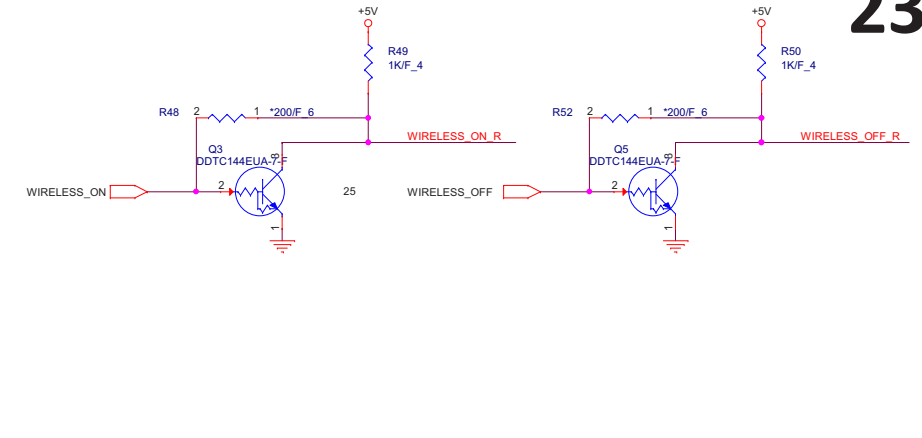
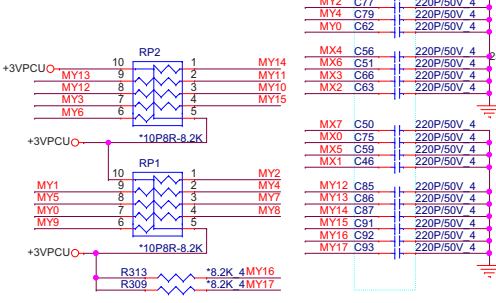
TP SMB DATA

KEYBOARD Con.

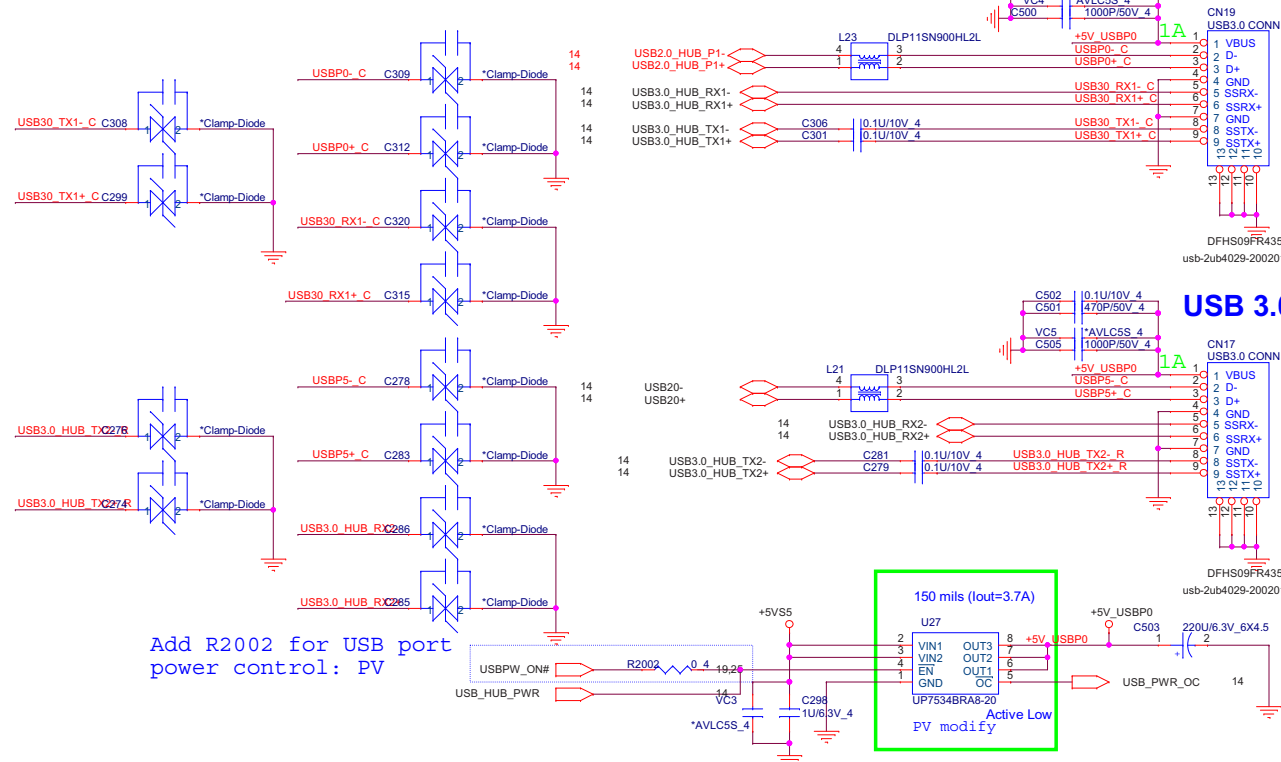
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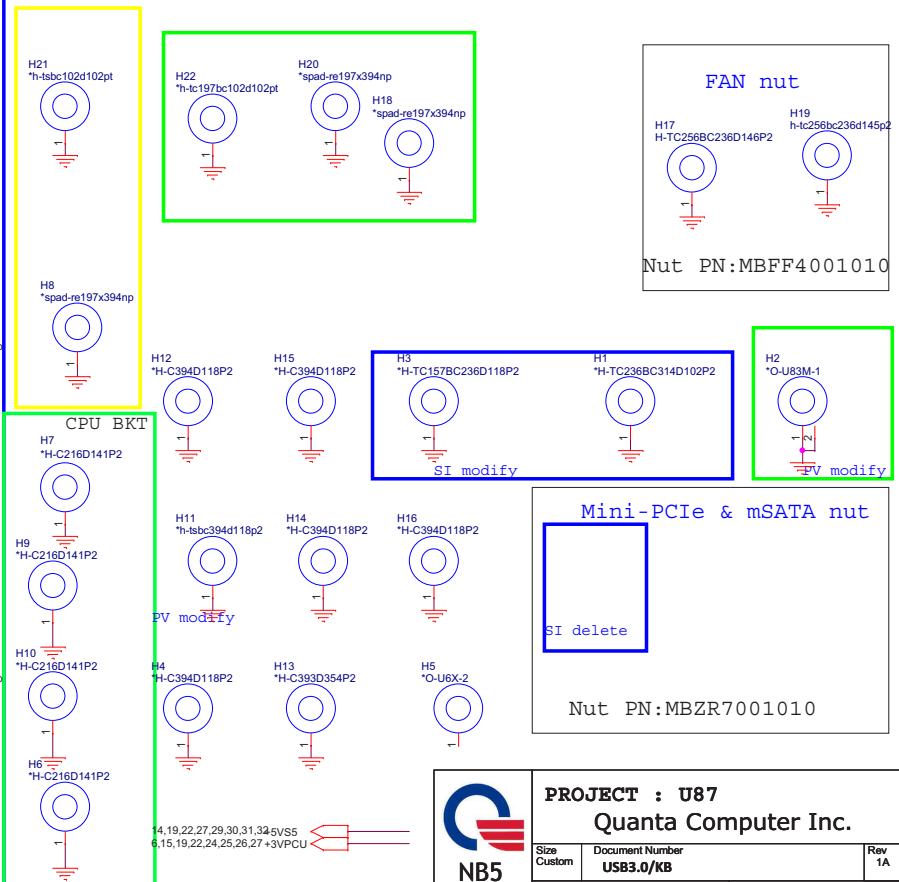
KEYBOARD PULL-UP



USB 2.0/3.0 Combo



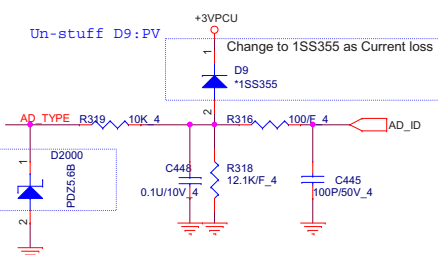
Hole



PROJECT : U87
Quanta Computer Inc.

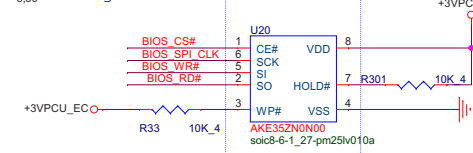
Size Custom	Document Number USB3.0/KB	Rev 1A
Date: Monday, November 18, 2013 Sheet 23 of 37		

adapter Type check

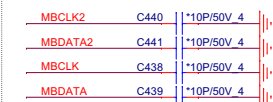


Vender	Size	P/N
WINBOND	128KB	W25X10CLSNIG(AKE35ZN0N00)
MXIC	128KB	MX25L1006EMI-10G(AKE35FN0Z02)
Socket		DFHS08FS023

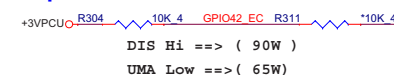
Change U20 from 1MB to 128KB:PV



Reserve for ENE Hold time issue



Adapter select for EC



+1.05V

4,9,11,12,13,14,15,17,18,19,20,21,22,23,24,32

6,15,19,22,23,24,26,27 +3VPCU

Change L27 to 0402: PV

4.7U/6.3V 6

for Battery charge/charge

for DDR Thermal IC

Stuff 22p on C454:PV

Un-Staff R322:PV

Reserve R2022:PV

Need Change New PN

KB3940QF A1

V18R

C464 0.1U/10V 4

C463 4.7U/6.3V 6

C449 0.1U/10V 4

C436 0.1U/10V 4

C437 0.1U/10V 4

C435 4.7U/6.3V 6

C434 0.1U/10V 4

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C203 0.1U/10V 4

C202 0.1U/10V 4

C201 0.1U/10V 4

C200 0.1U/10V 4

C199

27

DC/DC +3VS5/+5VS5

31

PV modify 0909

PV modify 0909

3.3 Volt +/- 5%
Continue current: 4A
Peak current: 6A
OCP minimum: 7.5A

+3VS5
+5VS5

2,9,11,14,15,22,24,28,30,31,32
14,19,22,23,29,30,31,32

25,28,31

Reserve for NB670 5V version.

PV modify 0911

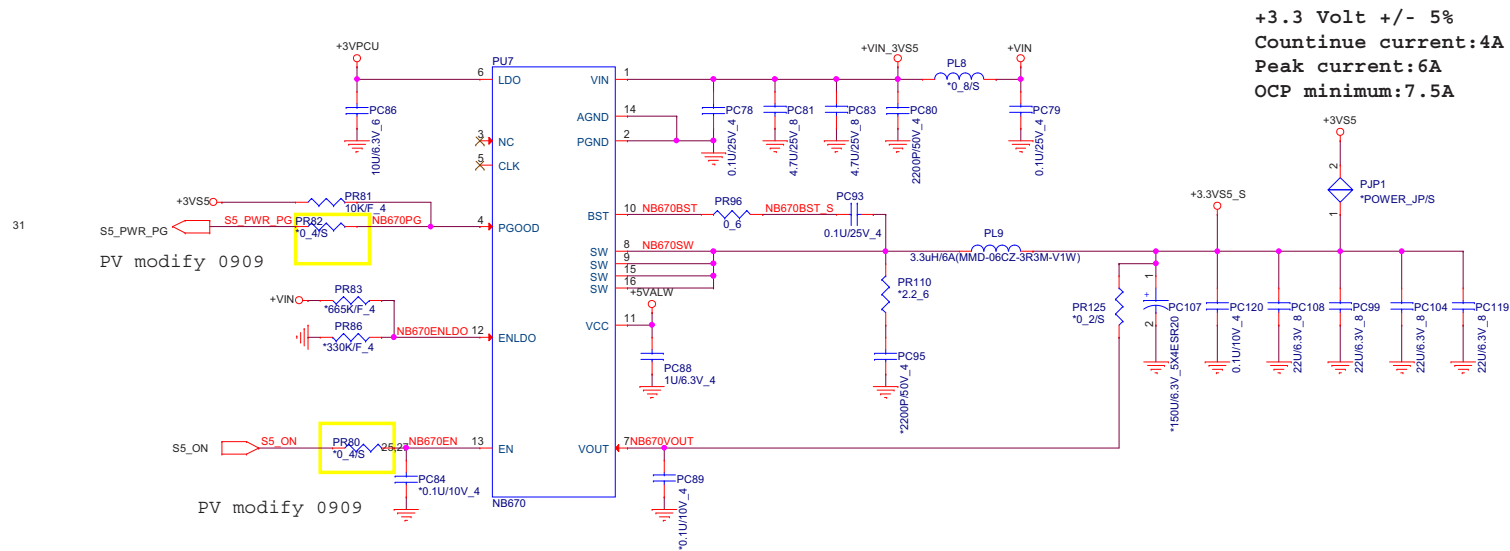
PV modify 0911

5 Volt +/- 5%
Continue current: 4A
Peak current: 6A
OCP minimum: 7.5A

Reserve for NB670 5V version.

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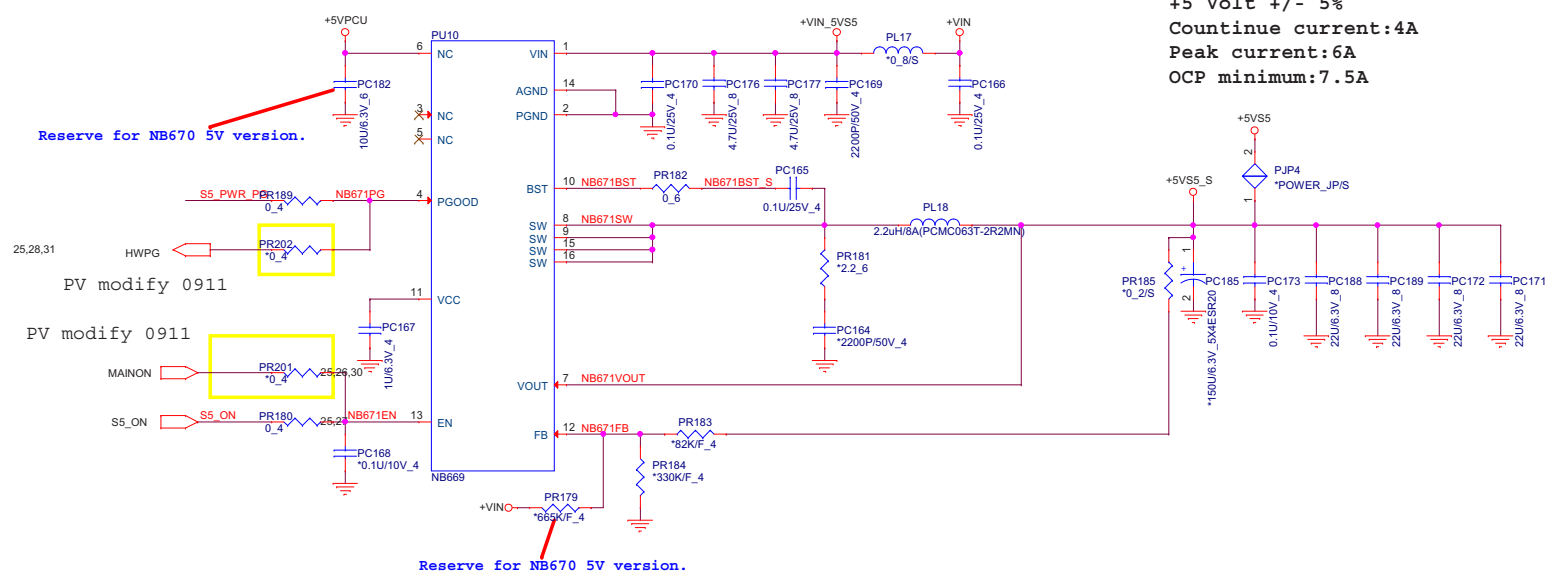
Size Custom	Document Number 3/5VPCU(NB670/NB669)	Rev 1A
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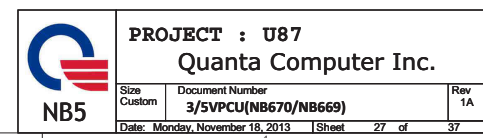
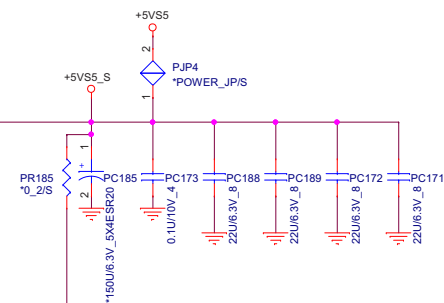
+3.3 Volt +/- 5%
Continue current:4A
Peak current:6A
OCP minimum:7.5A

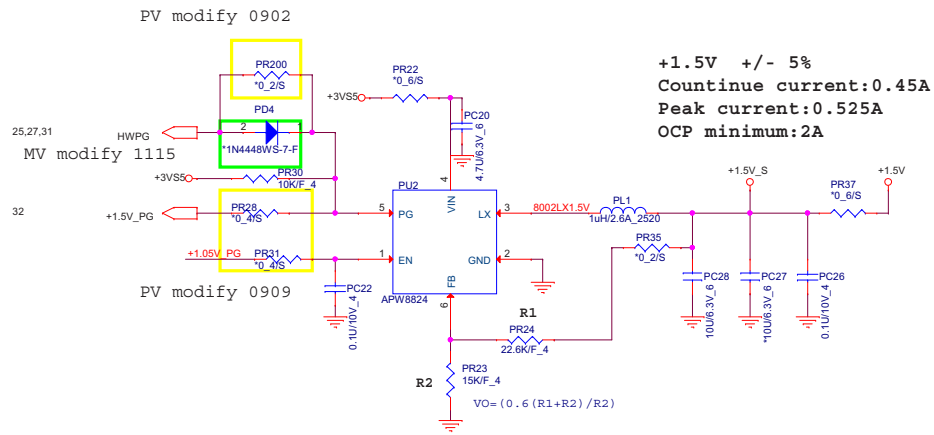
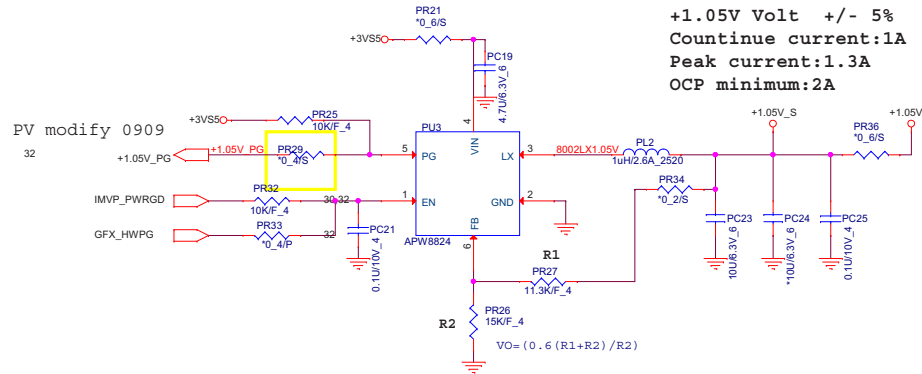


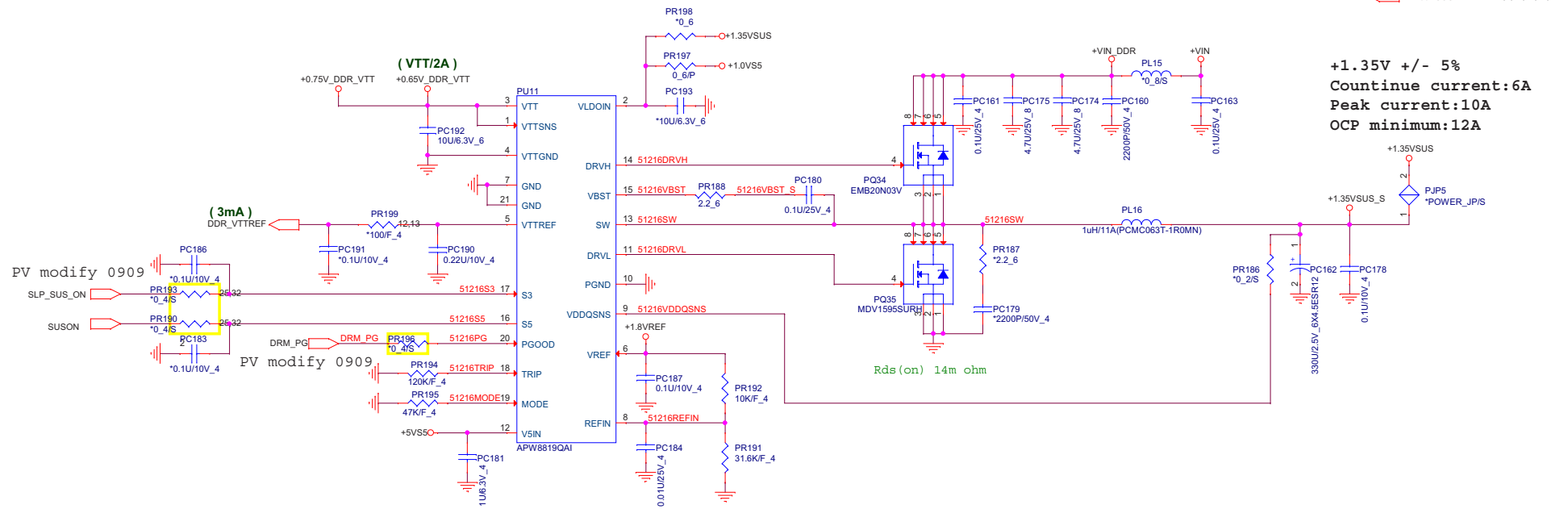
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14,19,22,23,29,30,31,32



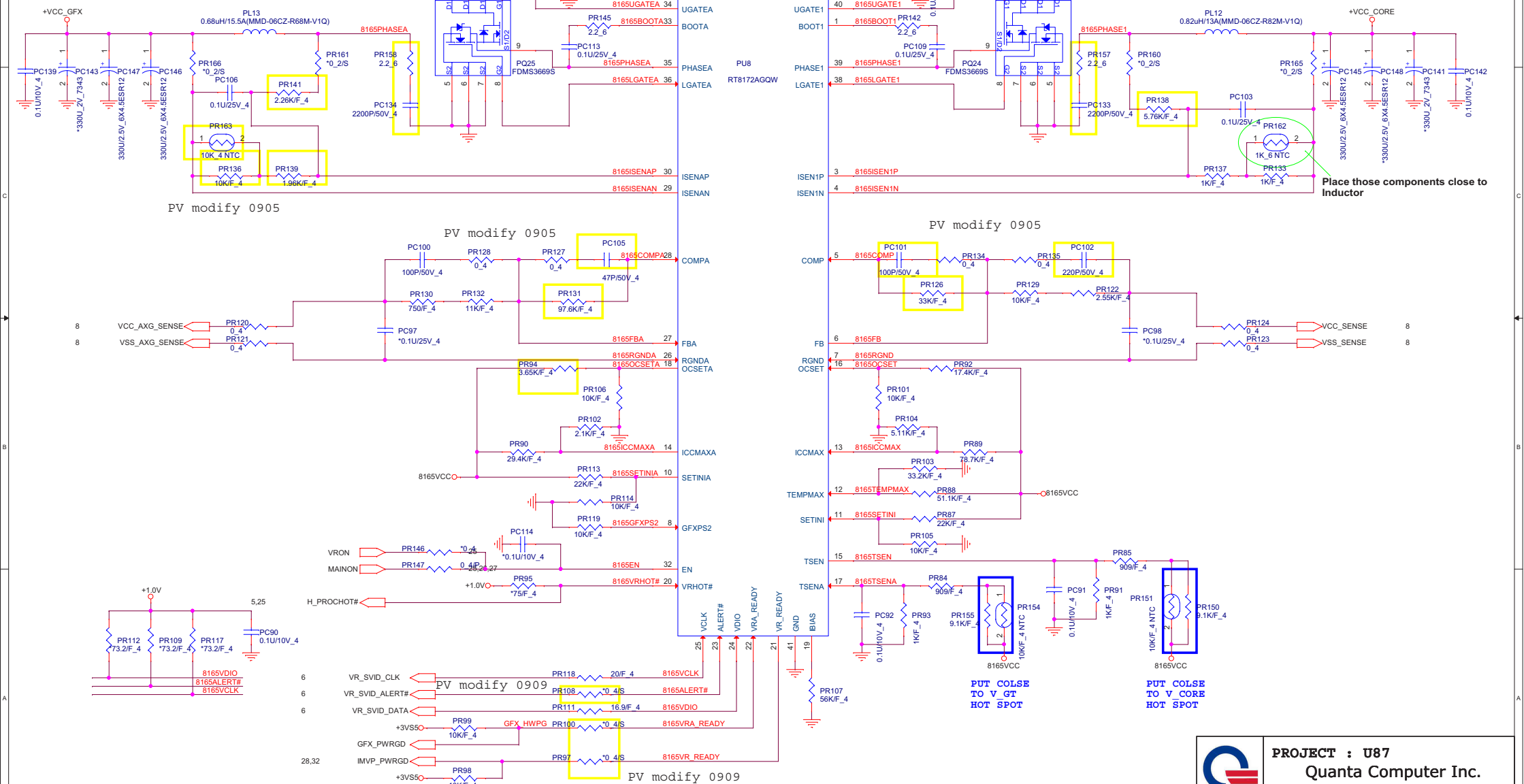
+5 Volt +/- 5%
Continue current:4A
Peak current:6A
OCP minimum:7.5A

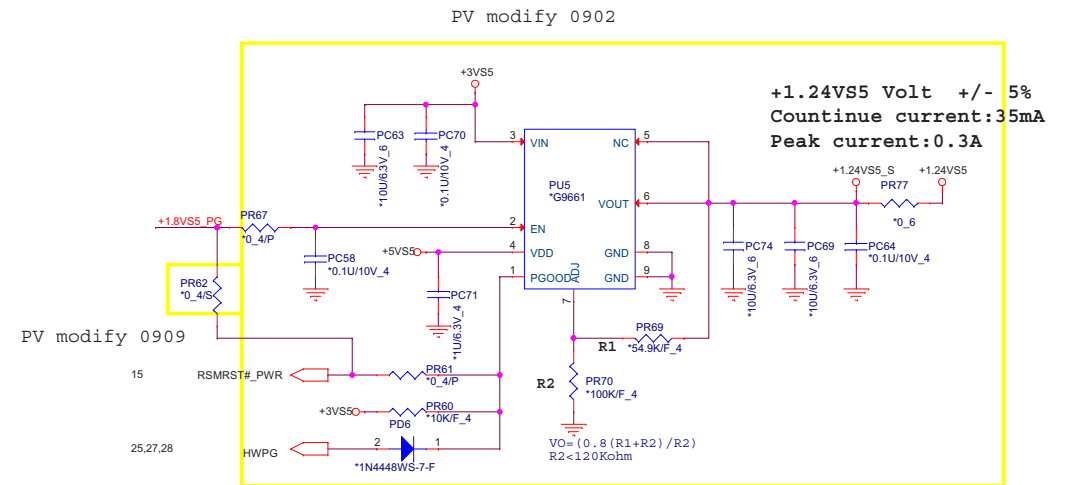
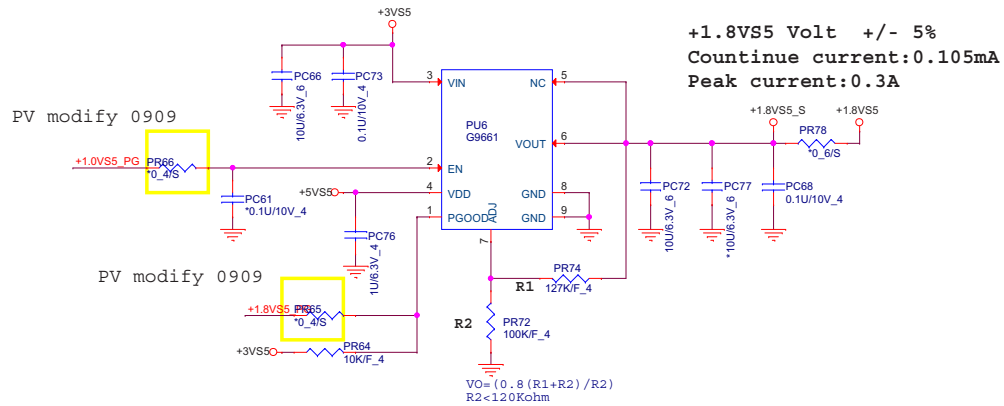
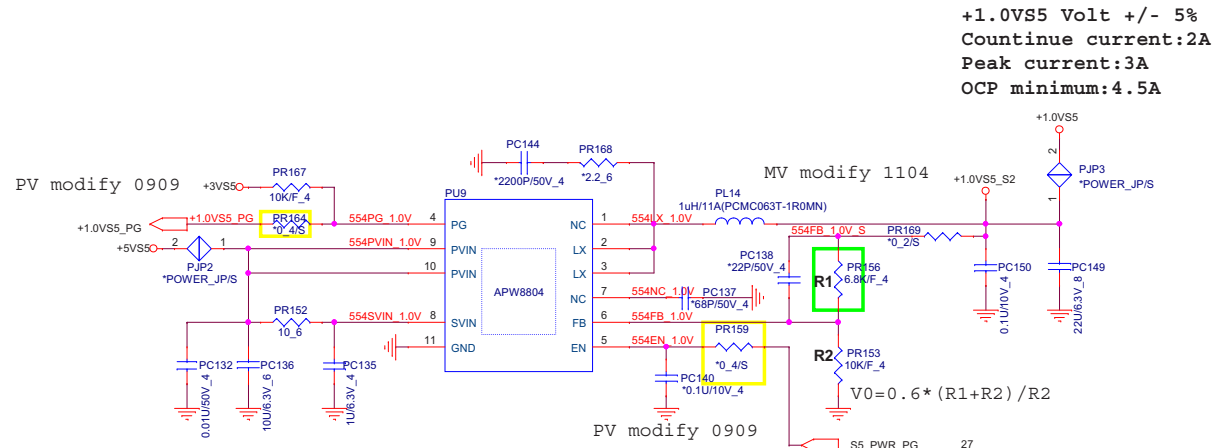


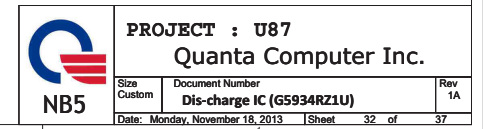




+GFXORE Volt +/- 5%
Countinue current:6A
Peak current:14A
OCP minimum:16.5A







USB3.0	Port Assignment	Power control pin
PORT0	USB HUB	

USB2.0	Port Assignment	Power control pin
PORT0	USB HUB	N/A
PORT1	Right side USB Daughter BD	USBPW_ON# (from EC)
PORT2	BT	N/A
PORT3	Camera	N/A

USB HUB	Port Assignment	Power control pin
USB30 PORT1	USB2.0/USB3.0 COMBO 1ST	USBPW_ON# (from EC)
USB30 PORT2	USB2.0/USB3.0 COMBO 2nd	USBPW_ON# (from EC)
USB30 PORT3	N/A	
USB30 PORT4	N/A	
USB20 PORT1	USB2.0/USB3.0 COMBO 1ST	USBPW_ON# (from EC)
USB20 PORT2	USB2.0/USB3.0 COMBO 2nd	USBPW_ON# (from EC)
USB20 PORT3	TS	TS_ON
USB20 PORT4		

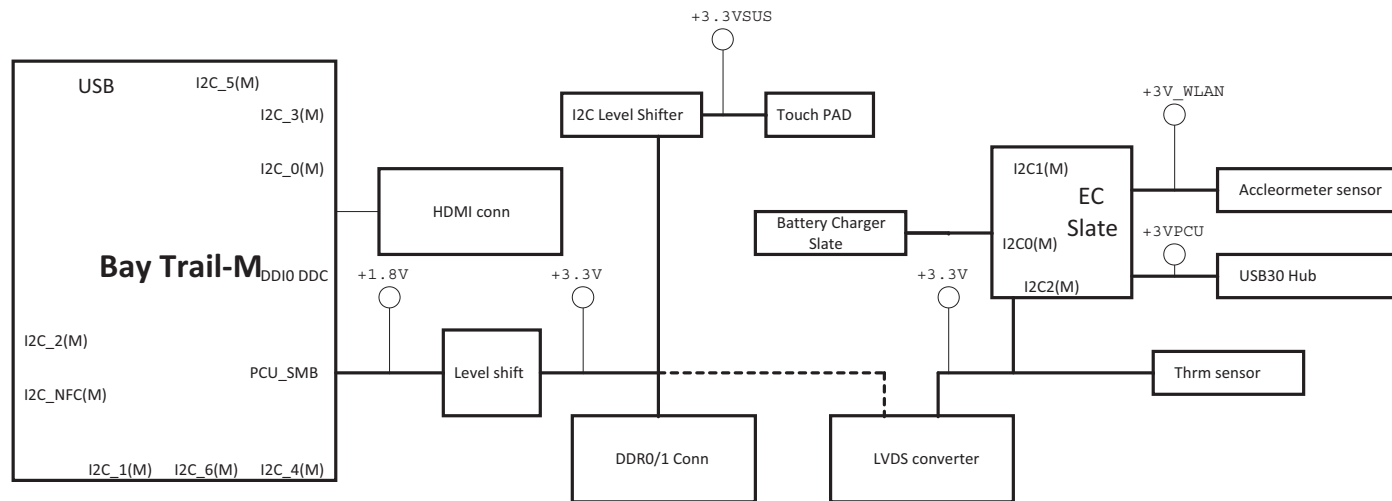
SATA Master	Port Assignment	Power control pin
SATA0	HDD	N/A
SATA1	ODD	ZERO_PWR_ODD

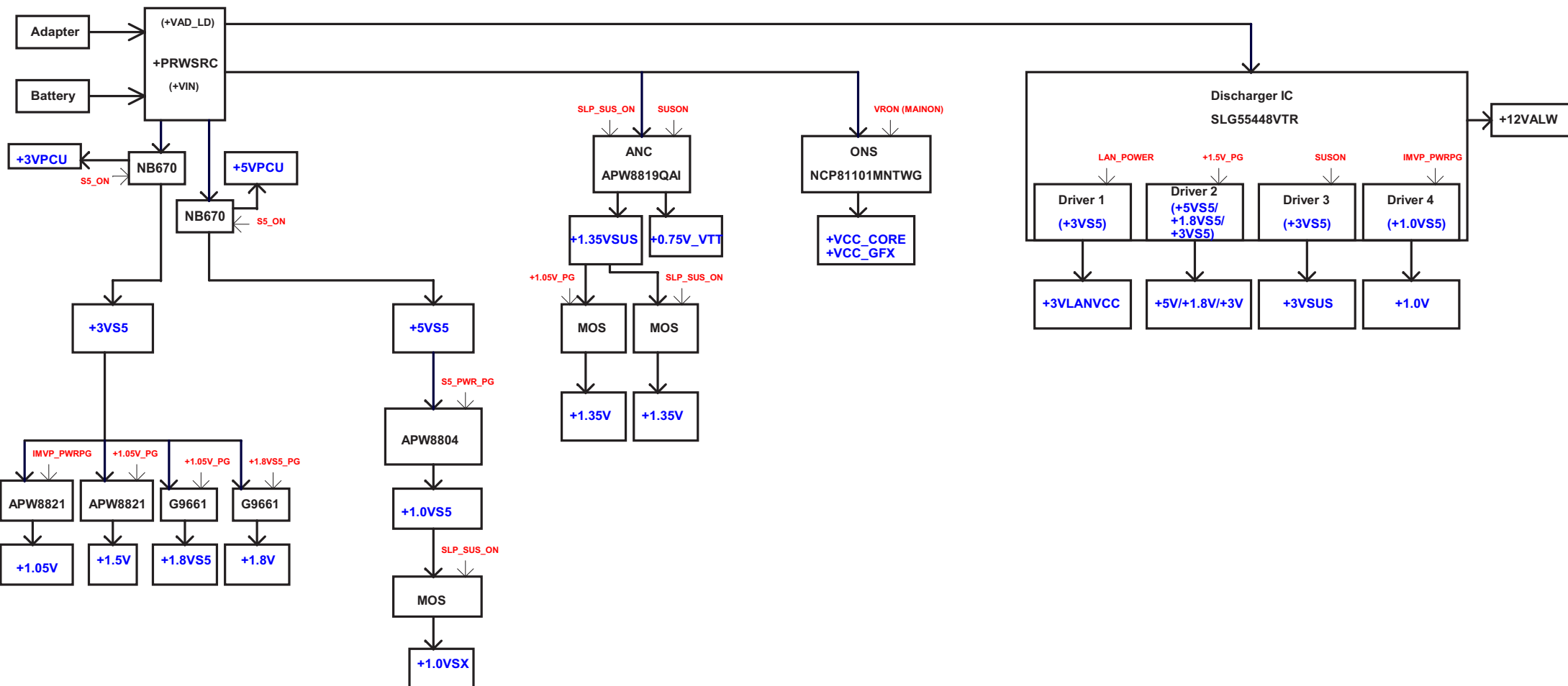
PCIE	Port Assignment	Control pin
PCIE 0	Card reader	
PCIE 1	WLAN	
PCIE 2	LAN	
PCIE 3	NC	

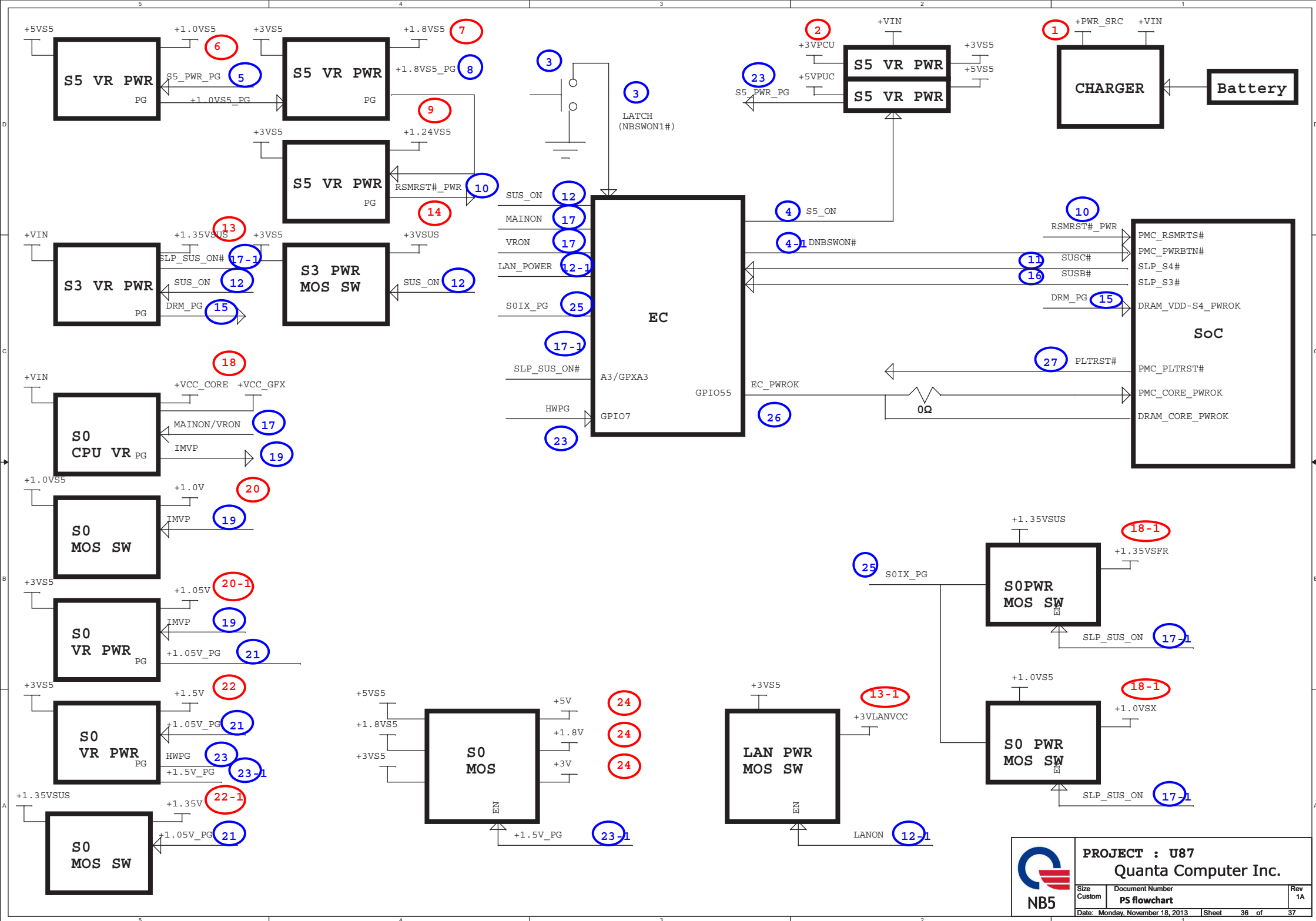


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	Quanta Computer Inc.		
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<small>Date: Monday, November 18, 2013 Sheet 37 of 37</small>			